REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicants cancel claims 9-10 and 19, and add new claims 21-23. Accordingly, claims 1-8, 11-18, and 19-23 remain pending in the application.

Reexamination and reconsideration are respectfully requested in view of the following Remarks.

OBJECTIONS TO DRAWINGS

By this Amendment, Applicants amend FIG. 2 to delete the reference numeral 128.

Regarding the objection to element 324 in FIG. 3, Applicants respectfully submit that it is indeed mentioned on page 10, line 13 of the specification.

Accordingly, Applicants respectfully request that the objections to the drawings be withdrawn.

35 U.S.C. §§ 102 and 103

The Office Action rejects: claim 13 under 35 U.S.C. § 102 over Callahan et al. "*The Garp architecture and C compiler*" ("Callahan"); claims 1, 4, 6- 8, 12 and 20 under 35 U.S.C. § 103 over Callahan in view of Page "Reconfigurable Processors" ("Page"); claims 2, 3, 5, and 15 under 35 U.S.C. § 103 over Callahan in view of Page and further in view of Miyamori et al. "REMARC: Reconfigurable multimedia array coprocessor" ("Miyamori"); claim 11 under 35 U.S.C. § 103 over Callahan in view of Page and further in view of Taylor U.S. Patent 5,857,109 ("Taylor"); and claims 14 and 16-18 under 35 U.S.C. § 103 over Callahan in view of Barat et al. "*Reconfigurable instruction set processor: An implementation platform for interactive multimedia applications*" ("Barat").

Applicants respectfully traverse all of these rejections for at least the following reasons.

Claim 13

Among other things, the unit of claim 13 includes a mechanism for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array.

Applicants respectfully submit that Callahan does not disclose a function unit including such a mechanism.

The Office Action cites Figure 1 and page 63, column 1, paragraph 9 of Callahan as supposedly disclosing such a feature as the "programmable wiring."

Applicants respectfully disagree.

Claim 13 recites that the mechanism reconfigures a plurality of intra-processor information paths to the array.

In contrast, page 63, column 1, paragraph 9 of Callahan discloses that "the Garp array is a two-dimensional ***array of CLBs interconnected by programmable wiring***." Thus, the cited text in Callahan merely discloses that the interconnections between the CLBs ***within*** the gate array are programmable, but it certainly does not disclose that the programmable wiring "reconfigures a plurality of ***intra***-processor information paths to the array." So Callahan merely discloses a conventional field programmable gate array (FPGA).

Accordingly, for at least these reasons, Applicants respectfully submit that claim 13 is patentable over Callahan.

Claim 1

Among other things, the coprocessor of claim 1 is connected to the processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

The Office Action states that Callahan discloses such a combination of features.

Applicants respectfully disagree

As explained above with respect to claim 13, Callahan merely discloses that the interconnections between the CLBs ***within*** the gate array are programmable, but

it certainly does not disclose that the programmable wiring "reconfigures a plurality of ***intra***-processor information paths to the array."

The Office Action does not allege that Page discloses such a feature, and of course it does not. So no combination of Callahan and Page could ever produce the coprocessor of claim 1.

Furthermore, Applicants respectfully traverse the proposed combination of Callahan and Page with respect to claim 1 as lacking any suggestion or motivation in the prior art. The text on page 1, paragraph 2 of Page that supposedly provides the motivation to modify Callahan has nothing at all to do with the proposed modification of Callahan. More specifically, nothing in the cited text indicates at all that modifying Callahan such that the coprocessor has an execution speed greater than that of the processor would "*effectively target the processor in a wide array of applications.*"

Accordingly, for at least these reasons, Applicants respectfully submit that claim 1 is patentable over the cited art.

Claims 4, 6-8 and 12

Claims 4, 6-8 and 12 all depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1.

Claim 20

Among other things, the method of claim 20 includes communicatively connecting the coprocessor to the processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

The Office Action states that Callahan discloses such a combination of features.

Applicants respectfully disagree

As explained above with respect to claims 13 and 1, Callahan merely discloses that the interconnections between the CLBs ***within*** the gate array are programmable, but it certainly does not disclose that the programmable wiring "reconfigures a plurality of ***intra***-processor information paths to the array."

The Office Action does not allege that Page discloses such a feature, and of

course it does not. So no combination of Callahan and Page could ever produce the method of claim 20.

Furthermore, Applicants respectfully traverse the proposed combination of Callahan and Page with respect to claim 20 as lacking any suggestion or motivation in the prior art, for reasons set forth above with respect to claim 1.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 20 is patentable over the cited art.

Claims 2, 3, 5 and 15

Claims 2, 3 and 5 depend from claim 1, and claim 15 depends from claim 13. Applicants respectfully submit that Miyamori does not remedy the shortcomings of Callahan as set forth above with respect to claim 13, and Callahan and Page as set forth above with respect to claim 1. Therefore, Applicants respectfully submits that claims 2, 3, 5 and 15 are patentable for at least the reasons set forth above with respect to claims 1 and 13, respectively, and for at least the following additional reasons.

Applicants respectfully traverse the proposed combination of Callahan and Page with Miyamori as lacking any suggestion or motivation in the prior art. The text on page 389, column 2, paragraph 3 of Miyamori that supposedly provides the motivation to modify Callahan has nothing to do with the proposed modifications. Tellingly, the exact same text and exact same supposed "motivation" are provided for modifying Callahan to include each of the various and diverse features cited in claims 2, 3 and 5. Clearly, this makes no sense, as the same supposed benefit cannot reasonably be argued to be provided separately by each of the various features of claims 2, 3 and 5!

Furthermore, with respect to claims 5 and 15, Applicants respectfully submit that the proposed modification of Callahan is contrary to M.P.E.P. § 2143.01 (V) and M.P.E.P. § 2143.01 (VI) as the entire point of Callahan is to provide total flexibility in the configuration of interconnections within the array, and this would be destroyed if inter-cell connections within the array were limited such that each cell of the array is connected only to cells whose column is the same and whose row is immediately

adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

Accordingly, for at least these additional reasons, Applicants respectfully submits that claims 2, 3, 5 and 15 are patentable over the cited art.

Claim 11

Claim 11 depends from claim 1. Applicants respectfully submit that Taylor does not remedy the shortcomings of Callahan and Page as set forth above with respect to claim 1. Therefore, Applicants respectfully submits that claim 11 is patentable for at least the reasons set forth above with respect to claim 1.

Claims 14 and 16-18

Claims 14 and 16-18 depend from claim 13. Applicants respectfully submit that Barat does not remedy the shortcomings of Callahan as set forth above with respect to claim 13. Therefore, Applicants respectfully submits that claims 14 and 16-18 are patentable for at least the reasons set forth above with respect to claim 13, and for at least the following additional reasons.

With respect to claim 17, the system includes an array program generator for generating array programs to be transmitted, and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to the mechanism to correspondingly update a current steady state connection pattern of the intra-processor information paths.

Applicants respectfully submit that Barat does not disclose transmitting a reconfigure signal to the mechanism to correspondingly update a current steady state connection pattern of the intra-processor information paths, and specifically does not disclose such a feature in page 483, columns 1, paragraph 3.

Accordingly, for at least this additional reason, Applicants respectfully submit that claim 17 is patentable over the cited art.

NEW CLAIMS 21-23

New claims 21-23 are deemed patentable over the cited art for at least the following reasons.

Claim 21

In the coprocessor of claim 21, the array is rectangular, wherein the periphery consists of those of said processing cells located in all of a first row, last row, first column and last column of said array, and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array.

None of the cited references, alone or in combination, disclose or suggest a mechanism reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array.

Claim 22

In the coprocessor of claim 22, the interface comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array.

None of the cited references, alone or in combination, disclose or suggest an interface that comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array.

Claim 23

The coprocessor of claim 23 includes a master cell for forwarding array programs to the processing cells of the two-dimensional array

None of the cited references, alone or in combination, disclose or suggest a coprocessor that includes such a master cell.

CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 1-8, 11-18, and 19-23 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this reply to charge payment or credit any overpayment (except for the issue fee) to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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Date: 21 May 2007

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